Changes Approved 2/8/05 MAL

Application No.: 10/033,007
Inventor: Mark Alan McAdams
Amendment dated October 4, 2004
Reply to Office Action of June 3, 2004

Amendments to the Specification:

Replace the Abstract with the following Abstract:

A system is provided for independently testing a circuit module embedded in a larger integrated circuit, such as a system ~~of~~ on a chip. The system uses essentially the circuit board level JTAG standard originally created to test chips mounted on a circuit board. The system provides a scan ring for serially scanning data to the inputs of the circuit module and for serially scanning out output from the circuit module. A test access port provides communications and control from an off-chip test interface to the scan rings.

Replace paragraph [1000] with the paragraph below:

[1000] The present invention relates to the field of integrated circuit design and testing and in particular, to testing of circuit ~~module~~ modules embedded in an integrated circuit.

Replace paragraph [1013] with the paragraph below:

[1013] Another option for testing embedded modules is to use a serial scan chain. In a serial scan chain, signals for the inputs of a design module are fed in sequentially though one of the pins on the chip. The signals are stored at multiple storage locations corresponding to inputs of the circuit module. As each new signal is input, the signals sequence through the storage locations corresponding to the circuit module inputs. When the proper signal is positioned at each of the inputs, the stored signals are captured and applied to the design module inputs. Similarly, the design module outputs are stored at each of the outputs, and then serially passed off the chip to a computer that reconstructs the output from the signals.

Replace paragraph [1016] with the paragraph below:

[1016] The present invention allows an individual circuit module to be tested independently of the rest of the chip. The invention uses a boundary scan register added to the circuit module to allow test vectors to be serially input through a ~~chip~~ the I/O pins of a chip and then applied to the circuit module inputs upon application of a control signal. The boundary scan register similarly allows the output of the circuit module to be stored and then serially scanned off the chip through chip I/O pins. Each of the module's internal connections can be made available for testing. The testing data and control are sent into the chip using a small number of pins that can be dedicated test pins or pins that function differently in test mode and in normal operation.

Replace paragraph [1032] with the paragraph below:

[1032] The JTAG protocol includes a series of commands used by a test designer to define and deliver the test vectors and to view the results. Each JTAG-capable chip samples the TMS line as the TCK signal cycles, and the TMS signal indicates whether the data on the TDI line corresponds to a command, which is to be routed to an internal command register, or to data, which is to be routed through the scan chain. The tester first sets up the instructions for all chips on a circuit board. Data is then scanned through the boundary scan registers according to the instructions provided.